AMENDEMENTS TO THE CLAIMS

1. (currently amended) A non-volatile memory comprising:

an array of non-volatile memory cells arranged in columns using bit lines; and

a verify circuit selectively coupled to the bit lines to determine if the memory cells have ~~a~~ an erase level that is within ~~a~~ an erase level window defined by first and second reference signals, the circuit generating an indication of one of under-erasure, erasure, or over-erasure in response to a position of the erase level with the erase level window.

2. (cancelled)

3. (currently amended) The non-volatile memory of claim 1 wherein the verify circuit comprises:

a first comparator with a reference input coupled to receive the first reference signal, and a second input coupled to the selected one of the bit lines; and

a second comparator with a reference input coupled to receive the second reference signal and a second input ~~is~~ coupled to the selected one of the bit lines.

4-5. (cancelled)

6. (original) The non-volatile memory of claim 1 wherein the memory cells comprise a plurality of floating gate memory cells.

7-44. (cancelled)

45. (new) The non-volatile memory of claim 1 wherein the indication is a "00" for under-erasure, a "10" for erasure, and a "11" for over-erasure.

46. (new) The non-volatile memory of claim 1 wherein the indication is a logical indication.

47. (new) The non-volatile memory of claim 1 wherein the erase level window indicates a current level.

48. (new) The non-volatile memory of claim 1 wherein the erase level window indicates a voltage level.

49. (new) The non-volatile memory of claim 47 wherein the first and second reference signals are current signals.

50. (new) The non-volatile memory of claim 48 wherein the first and second reference signals are voltage signals.

51. (new) A non-volatile memory comprising:

an array of non-volatile memory cells arranged in a row and column format such that the columns comprise bit lines including a selected bit line having a bit line current; and

a plurality of comparators for generating indication signals in response to a comparison of the bit line current with a plurality of reference currents each coupled to a comparator, each reference current indicating a different limit of an erase level window, each comparator generating an indication of one of under-erasure, erasure, or over-erasure in response to the comparison.

52. (new) The non-volatile memory of claim 51 wherein the plurality of comparators comprise a first comparator that compares the bit line current to a lower limit reference current and a second comparator that compares the bit line current to an upper limit reference current.

53. (new) The non-volatile memory of claim 52 wherein a bit line current that is less than the upper limit reference current and greater than the lower limit reference current is a current indicating erasure.

54. (new) A non-volatile memory comprising:

an array of non-volatile memory cells arranged in a row and column format such that the columns comprise bit lines including a selected bit line having a bit line current; and

a plurality of comparators for generating indication signals in response to a comparison of a voltage that is representative of the bit line current with a plurality of reference voltages each coupled to a comparator, each reference voltage indicating a different limit of an erase level window, each comparator generating an indication of one of under-erasure, erasure, or over-erasure in response to the comparison.